UG 1 6 2005

Discoosure Statement Transmittal

Patent Docket No.: NVID-P001125

	his transmittal of the below described document in Postage and addressed to the Commissioner of P	atents, P. O. Box 1450, Alexand		
Date of Deposit: 8/12/0	Name of Person Making the Deposit: Mrz (AS/7)	Signature of the Person Making the Deposit:	7 CashH	
Inventor(s):	IN THE UNITED STATES PAT Schieck et al.			
Application No.:	10/789,637	Group Art Unit: 281	2	
Filed:	February 27, 2004	Examiner: Not	yet assigned.	
Title:	A FLIP CHIP SEMICONDUCTOR DI	E INTERNAL SIGNAL A	CCESS SYSTEM A	AND
Commissioner of P. O. Box 1450 Alexandria, VA 2 Sir:				
Oil.	Information Disclosur	e Statement Transmittal		
	ewith is the following:			
	vings, totalingsheets.			
	awings, totaling sheets. If for PTO Consideration		•	
	Disclosure statement (2 sheets)			
	Disclosure statement (2 sheets)	1	•	
X Form 1449	Distribute statement and late iming to			
Petition for	Extension of Time			
Other:	,			
Fee Calculati	ion (for other than a small entity)			
Fee Items			Fee Rate	Total
	nsion of Time (fee calculated elsewhere		\$.00	
Information Disclosure Statement, late filing			\$180.00	

PAYMENT OF FEES

- 1. The full fee due in connection with this communication is provided as follows:
- The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085.

 A duplicate copy of this authorization is enclosed.
- [] A check in the amount of \$
- [X] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Other: Total Fees

0.00

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

Two North Market Street, Third Floor San Jose, California 95113 (408) 938-9060

Customer No: 000041066

Respectfully submitted,

Date: Hy S, Zoros

Anthony C. Murabito Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No.: NVID-P001125 ify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450, on the below date of deposit. Signature of the Person Name of Person B/12/05 Making the Deposit: Date of Making the Deposit: Deposit: Confirmation No.: 7655 Schieck et al. Inventor(s): 2812 Group Art Unit: 10/789,637 Application No.: Not yet assigned. Examiner: February 27, 2004 Filed: A FLIP CHIP SEMICONDUCTOR DIE INTERNAL SIGNAL ACCESS SYSTEM AND Title: METHOD Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Certification for PTO Consideration of an Information Disclosure Statement Sir: (Under 37 CFR §1.97) Consideration of the enclosed Information Disclosure Statement is requested. 1. This certification is being made for this information disclosure statement [X] accompanying this certification [] Filed _ 2. Thereby certify that: X___ Each item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement. No item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, or, to the knowledge of the person signing certification after making reasonable inquiry, was known to any individual designated in §1.56(c) more than three months prior to the filing of the statement. 3. The person making this certification is a person who is substantively involved in the preparation or prosecution of the application, and who is associated with the inventor, with the assignee, or with anyone to whom there is an [x] obligation to assign the application (37 C.F.R. 1.56 (c)) and who signs below. the inventor(s) who signs below [] the practitioner who signs below on the basis of the information: [] [] supplied by the inventors [] supplied by an individual designated in § 1.56(c) [] in the practitioners file

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

Two North Market Street, Third Floor San Jose, California 95113 (408) 938-9060 Customer No: 000041066

Respectfully submitted,

Date: Avs S, ZOS

Anthony C. Murabito Reg. No. 35,295



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NVID-P001125

Schiek et al.

Group Art Unit: 2812

Filed:

February 27, 2004

Examiner:

Not yet assigned.

Application No.:

10/789,637

Confirmation No.: 7655

Title:

A FLIP CHIP SEMICONDUCTOR DIE INETNRAL SIGNAL ACCESS SYTEM AND METHOD

Commissioner of Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:					
Publ./Pat. No.	Publ./Pat. Title	Grant Date			
US 2001/0010356	. THROUGH-THE-SUBSTRATE INVESTIGATION OF FLIP-CHIP IC'S	Aug. 2, 2001			
US 2001/0006233	SEMICONDUCTOR DEVICES HAVING BACKSIDE PROBING CAPABILITY	Jul. 5, 2001			
US 2003/0119297	METAL REDISTRIBUTION LAYER HAVING SOLDERABLE PADS AND WIRE BONDABLE PADS	Jun. 26, 2003			
5,258,648	COMPOSITE FLIP CHIP SEMICONDUCTOR DEVICE WITH AN INTERPOSER HAVING TEST CONTACT FO ALONG ITS PERIPHERY	•			
6,081,429	TEST INTERPOSER OR USE WITH BALL GRID ARRAY PACKAGES ASSEMBLIES AND BALL GRID ARRAY PACKAGES INCLUDING SAME AND METHOL	Jun. 27, 2000 OS			
6,686,615	FLIP-CHIP TYPE SEMICONDUCTOR DEVICE FOR REDUCING SIGNAL SKEW	Feb. 3, 2004			
6,307,162	INTEGRATED CIRCUIT WIRING	Oct. 23, 2001			

FOREIGN DOCUMENTS

DE 195 15 591 A1

PRUUNGSANTRAG GEM

Oct. 19 1995

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP

Two North Market Street, Third Floor San Jose, California 95113 (408) 938-9060

Customer No: 000041066

Respectfully submitted,

Anthony C. Murabito Reg. No. 35,295



Attorney Docket No.: NVID-P001125

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s):

Schieck et al.

Confirmation No.: 7655

Application No.:

10/789,637

Group Art Unit: 2812

Filed:

February 27, 2004

Examiner:

Not yet assigned.

Title:

A FLIP CHIP SEMICONDUCTOR DIE INTERNAL SIGNAL ACCESS SYSTEM AND

METHOD

Form 1449

U.S. Patent Documents

Examiner						Sub-	Filing
Initial	No.	Publ./Patent No.	Date	Patentee	Class	class	Date
	Α	2001/0010356	8/2/01	Talbot et al.	250	307	2/10/01
	В	2001/0006233	7/5/01	Vallett	257	48	1/29/01
	C	2003/0119297	6/26/03	Am et al.	438	612	1/27/03
	D	5,258,648	11/2/93	Lin	257	778	11/27/92
	E	6,081,429	6/27/00	Barrett	361	767	1/20/99
	F	6,686,615	2/3/04	Cheng et al.	257	208	8/20/02
	G	6,307,162	10/2/01	Masters et al.	174	262	12/9/96
	Н		,				
	J		-				
	K			·			

Foreign Patent or Published Foreign Patent Application

Examiner		Document	Publication	Country or	,	Sub-	Trans	lation
Initial	No.	No.	Date	Patent Office	Class	class	Yes	No
	L	19515591	10/19/95	DE	HOL	23/525		Х
	М							
	N							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
•	R	
-	S	
	T	
Examiner	ı	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.